|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **U.S.N.** |  |  |  |  |  |  |  |  |  |  |

**B.M.S. College of Engineering, Bengaluru-560019**

**Autonomous Institute Affiliated to VTU**

**July / August 2019 Supplementary Examinations**

|  |  |
| --- | --- |
| **Programme: B.E.** | **Semester : III** |
| **Branch : Computer Science and Engineering** | **Duration: 3 hrs.** |
| **Course Code : 15CS3DCCOA** | **Max Marks: 100** |
| **Course Title : Computer Organization and Architecture** | **Date: 01.08.2019** |

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.

2. Missing data, if any may suitably assumed.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice. |  |  | **UNIT - I** |  |
| 1 | a) | Describe addressing mode. List any four addressing modes and explain with example. | **10** |
|  | b) | Convert the following pairs of decimal numbers to 5-bit 2’s complement numbers, then add them   1. -5 and 7 2. -3 and -8 | **06** |
|  | c) | For the following processor, calculate the performance (or time required to execute).  Clock rate = 800 MHz  Number of instructions executed = 1000  Average number of steps needed per machine instruction = 20 | **04** |
|  |  | **UNIT - II** |  |
| 2 | a) | With neat diagram explain centralized and distributed bus arbitration scheme. | **10** |
|  | b) | By applying program – controlled Input-output organization develop assembly level language program that reads one line from keyboard, stores it in memory buffer and echoes it back to the display. Consider memory buffer starts from the memory location with name as “LOC”, terminating character of the line input from keyboard as hexadecimal value ‘OD’ and following registers are available in keyboard and display interface.  DATAIN DATAOUT   |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  | SOUT | SIN |     STATUS | **10** |
|  |  | **OR** |  |
| 3 | a) | With a neat diagram explain the Universal Serial Bus Architecture. | **10** |
|  | b) | Design a 8-bit parallel interface circuit. Show you design with neat diagram and describe. | **10** |
|  |  | **UNIT - III** |  |
| 4 | a) | With neat diagram explain Virtual Memory Address Translation. | **10** |
|  | b) | 1024x1024 array of 32-bit numbers is to be normalized as follows. For each column the largest element is found and all elements of the column are divided by this maximum value. Assume that each page in the virtual memory consists of 4Kbytes and that 1Mbytes of the main memory are allocated for storing data during this computation. Suppose that it takes 40 ms to load a page from the disk to the main memory when a page fault occurs (assume that when we start, the main memory is empty ).  **(i)** How many page faults would occur if the elements of the array are stored in column order in the virtual memory?  **(ii)** Estimate the total time needed to perform this normalization for the arrangement **(i)**. | **10** |
|  |  | **OR** |  |
| 5 | a) | Design a memory chip of size 1K x 1. Arrange the memory cells as a matrix of 32-bits x 32-bits. Show your design with neat diagram. | **10** |
|  | b) | A a cache is organized in the direct-mapped manner with the following parameters:  Main Memory size 64K words.  Cache size 1K words  Block size 128 words   1. How many bits are there in main memory address? 2. How many bits are there in each of the TAG, BLOCK and WORD fields? | **05** |
|  | c) | A disk unit has 24 recording surfaces and has a total of 14,000 Cylinders. There is an average of 400 sectors per track, each sector contains 512 bytes of data.   1. What is the maximum number of bytes that can be stored in this disk unit? 2. What is the data transfer rate in bytes per second at a rotational speed of 7200 rpm?   (Note: rpm=Revolutions per minute.) | **05** |
|  |  |  |  |
|  |  | **UNIT - IV** |  |
| 6 | a) | 1. Explain single and double precision IEEE floating point number formats. 2. Represent (0.625)10 in single and double precision IEEE floating point numbers formats. | **10** |
|  | b) | Multiply (+22)(Multiplicand) with Multiplier(-6) using Booth’s  Algorithm Method. Consider 6-bit number representation. | **05** |
|  | c) | Multiply 110101 (Multiplicand) with 011011 (Multiplier) using Bit-Pair Recoding Method | **05** |
|  |  | **UNIT - V** |  |
| 7 | a) | Using single bus organization, write complete control sequence for execution of the instruction Add (R3), R1 ; *R1* | **10** |
|  | b) | Explain with block diagram the basic organization of a micro programmed Control unit | **10** |

\*\*\*\*\*\*\*